Claims

We claim:

1. A frequency-adjustable oscillator suitable for digital signal clock synchronization, the oscillator comprising:

a crystal oscillator circuit for generating a driving signal and having a voltage-variable control input for adjusting a frequency of the driving signal, the crystal oscillator circuit including a voltage variable capacitive element responsive to the control input, an AT-cut quartz resonator operably linked to the voltage variable capacitive element, and a gain stage for energizing the quartz resonator;

a phase detector circuit for generating a phase offset signal;

a filter which operates on the phase offset signal to produce a VCO control signal;

a voltage controlled oscillator circuit operably linked to the filter and responsive to the VCO control signal for generating an analog controlled-frequency signal;

a frequency divider circuit having a preselected divider ratio operably linked between the voltage controlled-frequency oscillator circuit and the phase detector circuit for generating a reduced frequency feedback signal in response to the controlled-frequency signal,

the phase detector circuit being responsive to the feedback signal and the driving signal such that the phase offset signal varies according to a phase difference between the feedback signal and the driving signal;

a double-sided package including a platform having a central portion and an outer portion, sidewalls extending substantially upwardly and substantially downwardly from the outer portion of the platform;

the upwardly extending sidewalls and the platform forming a first cavity adapted to receive and electrically connect the quartz resonator;

the downwardly extending sidewalls and the platform forming a second cavity adapted to receive and electrically connect at least one electronic component; and

a cover coupled with the first cavity defining a hermetic environment for containing the quartz resonator.

2. The oscillator according to claim 1 wherein the voltage variable capacitive element includes a discrete varactor received in the second cavity and operably linked to the quartz resonator.

3. The oscillator according to claim 1 wherein the voltage controlled oscillator circuit is resident on an electronic component received in first cavity.

4. The oscillator according to claim 1 wherein the following elements are received in said second cavity the gain stage,
the phase detector circuit, the voltage controlled oscillator circuit, and the frequency divider circuit.

5. The oscillator according to claim 1 wherein the following elements are integrated in a single semiconductor chip received in said second cavity:

the gain stage,

the phase detector circuit,

the voltage controlled oscillator circuit, and

the frequency divider circuit.

6. The oscillator according to claim 1 further comprising a laminate substrate coupled with the second cavity.

7. The oscillator according to claim 6 wherein said platform has a second-cavity side, and at least one electronic component is mounted on the second-cavity side and at least one electronic component is mounted on said laminate substrate.

8. The oscillator according to claim 6 wherein the laminate substrate includes a side castellation.

9. The oscillator according to claim 6 wherein the laminate substrate is multi-layered and includes a buried inductor.

10. The oscillator according to claim 1 further comprising a printed circuit board coupled with the second cavity, the printed circuit board having a cavity facing surface adapted to receive at least one electronic component and an outward facing surface having a plurality of integral contacts adapted to facilitate electrical surface mountable connection to an electrical device.

11. The oscillator according to claim 1 wherein the AT-cut quartz resonator is tunable and the second cavity includes contacts conductively linked to the resonator for tuning.

12. The oscillator according to claim 1 wherein the controlled-digital logic output has a nominal operating frequency of 622.08 Megahertz and an Absolute Pull Range of at least 50 ppm.

13. The oscillator according to claim 1 wherein the controlled frequency signal has a nominal operating frequency of about 644.531 Megahertz and an Absolute Pull Range of at least 50 ppm.

14. The oscillator according to claim 1 wherein the controlled frequency signal has a nominal operating frequency of about 666.514 Megahertz and an Absolute Pull Range of at least 50 ppm.

15. The oscillator according to claim 1 wherein the controlled frequency signal has a nominal operating frequency of about 669.326 Megahertz and an Absolute Pull Range of at least 50 ppm.

16. The oscillator according to claim 1 further comprising a sinewave-to-logic level translator circuit operably linked to the voltage controlled oscillator for generating a digital output signal having substantially the same frequency as the controlled-frequency signal.

17. The oscillator according to claim 16 wherein the translator circuit is a differential receiver adapted to generate the digital output signal at voltage levels conventional for positive-referenced emitter coupled logic (PECL).

18. The oscillator according to claim 1 having a substantially rectangular footprint of about 5 millimeters by 7 millimeters.

19. The oscillator according to claim 1 having a footprint of an area less than about 40 square millimeters.

20. The oscillator according to claim 1 wherein the quartz resonator is configured to operate in fundamental mode.

21. The oscillator according to claim 1 wherein the crystal oscillator circuit further includes temperature compensation.

22. A frequency-adjustable oscillator suitable for digital signal clock synchronization, the oscillator comprising:

a double-sided package including a platform having a central portion and an outer portion, sidewalls extending substantially upwardly and substantially downwardly from the outer portion of the platform;

the upwardly extending sidewalls and the platform forming a first cavity adapted to receive and electrically connect a quartz resonator;

the downwardly extending sidewalls and the platform forming a second cavity adapted to receive and electrically connect at least one electronic component;

a crystal oscillator circuit for generating a driving signal and having a voltage-variable control input for adjusting a frequency of the driving signal, the crystal oscillator circuit including a voltage variable capacitive element responsive to the control input, an AT-cut quartz resonator received in the first cavity and operably linked to the voltage variable capacitive element, and a gain stage for energizing the quartz resonator;

a phase detector circuit for generating a phase offset signal;

a filter which operates on the phase offset signal to produce a VCO control signal;

a voltage controlled oscillator circuit operably linked to the filter and responsive to the VCO control signal for generating an analog controlled-frequency signal;

a frequency divider circuit having a preselected divider ratio operably linked between the voltage controlled-frequency oscillator circuit and the phase detector circuit for generating a reduced frequency feedback signal in response to the controlled-frequency signal,

the phase detector circuit being responsive to the feedback signal and the driving signal such that the phase offset signal varies according to a phase difference between the feedback signal and the driving signal;

a sinewave-to-logic level translator circuit operably linked to the voltage controlled oscillator for generating a digital output signal having substantially the same frequency as the controlled-frequency signal;

a cover coupled with the first cavity defining a hermetic environment for containing the quartz resonator.

23. The oscillator according to claim 22 wherein the following elements are integrated in a single semiconductor chip received in said second cavity:

the gain stage,

the phase detector circuit,

the voltage controlled oscillator circuit, and

the frequency divider circuit.

24. A frequency-adjustable oscillator suitable for digital signal clock synchronization, the oscillator comprising:

a temperature sensor;

a temperature compensation logic operably linked to the temperature sensor for generating a capacitance adjustment;

a variable capacitance circuit having and being responsive to a control input for providing a variable capacitive load, the variable capacitance circuit also being responsive to the capacitance adjustment;

a resonator gain stage;

a quartz resonator operably linked to the gain stage and the variable capacitance circuit for generating a driving signal;

a phase detector circuit for generating a phase offset signal;

a filter which operates on the phase offset signal to produce a VCO control signal;

a voltage controlled oscillator circuit operably linked to the filter and responsive to the VCO control signal for generating an analog controlled-frequency signal;

a frequency divider circuit having a preselected divider ratio operably linked between the voltage controlled-frequency oscillator circuit and the phase detector circuit for generating a reduced frequency feedback signal in response to the controlled-frequency signal,

the phase detector circuit being responsive to the feedback signal and the driving signal such that the phase offset signal varies according to a phase difference between the feedback signal and the driving signal;

a double-sided package including a platform having a central portion and an outer portion, sidewalls extending substantially upwardly and substantially downwardly from the outer portion of the platform;

the upwardly extending sidewalls and the platform forming a first cavity adapted to receive and electrically connect the quartz resonator;

the downwardly extending sidewalls and the platform forming a second cavity adapted to receive and electrically connect at least one electronic component; and

a cover coupled with the first cavity defining a hermetic environment for containing the quartz resonator.

25. The oscillator according to claim 24 wherein the following elements are integrated in a single semiconductor chip received in said second cavity:

the temperature sensor,

the temperature compensation logic,

the variable capacitance circuit,

the gain stage,

the phase detector circuit,

the voltage controlled oscillator circuit, and

the frequency divider circuit.

26. The oscillator according to claim 24 further comprising a laminate substrate coupled with the second cavity.

27. The oscillator according to claim 24 further comprising a printed circuit board coupled with the second cavity, the printed circuit board cover having a cavity facing surface adapted to receive at least one electronic component and an outward facing surface having a plurality of integral contacts adapted to facilitate electrical surface mountable connection to an electrical device.